DACSINE PAGE 1

1 ;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

2 ;

3 ; Author : ADI - Apps www.analog.com/MicroConverter

4 ;

5 ; Date : 5 November 2001

6 ;

7 ; File : DACsine.asm

8 ;

9 ; Hardware : ADuC834

10 ;

11 ; Description : DAC outputs a sine wave 1.1kHz to pin 12.

12 ; Rate calculations assume an 32.768kHz crystal

13 ; producing a core frequency of 12.58MHz.

14 ;

15 ;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

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17 $MOD834 ; Use 8052&ADuC834 predefined symbols

18

00B4 19 LED EQU P3.4 ; P3.4 drives red LED on eval board

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22 ; BEGINNING OF CODE

---- 23 CSEG

24

0000 25 ORG 0000h

26

0000 75D700 27 MOV PLLCON, #00H ; set core frequency to 12.58MHz

28

0003 75FD03 29 MOV DACCON,#03h ; Configure DAC with

30 ; DAC on

31 ; 12bit

32 ; o/p @ pin 10

33 ; Range 0-> Vref (2.5V internal ref)

34

0006 75FC08 35 MOV DACH,#08h ; DAC to mid-scale (1.25V) to start

0009 75FB00 36 MOV DACL,#00h ; transmissions from mid-scale

37

38

000C 901000 39 MOV DPTR, #TABLE

40

000F E4 41 STEP: CLR A ; 1

0010 93 42 MOVC A,@A+DPTR ; get high data byte from table.. 2

0011 F5FC 43 MOV DACH,A ; ..and move it into DAC register 1

0013 A3 44 INC DPTR ; move on to get low byte 2

45

0014 E4 46 CLR A ; 1

0015 93 47 MOVC A,@A+DPTR ; get low data byte from table.. 2

0016 F5FB 48 MOV DACL,A ; ..and update DAC output 1

0018 A3 49 INC DPTR ; move on for next data point 2

50

0019 E582 51 MOV A, DPL ; Check if DPL=80h, if so then the 1

001B B480F1 52 CJNE A,#80h,STEP ; table has been outputted and we 2

001E 901000 53 MOV DPTR, #TABLE ; should reset the DPTR to 1000h

0021 B2B4 54 CPL LED ; and start outputting data again

55

0023 80EA 56 JMP STEP ;

57

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58 ; Numbers at right in the above loop represent the number of machine

59 ; cycles for each instruction. The typical loop ends after the CJNE

60 ; command thus requiring 15 machine cycles.

61 ; With a 12.583MHz master clock, a machine cycle takes 0.953us to

62 ; execute, so the above loop takes 14.3us to update each data point.

63 ; Since there are 64 data points in the below sine lookup table,

64 ; this results in a 915us period, i.e. a 1.1kHz frequency.

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66 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

67 ; SINE LOOKUP TABLE

1000 68 ORG 01000h

69

1000 70 TABLE:

71

1000 07FF 72 DB 007h, 0FFh

1002 08C8 73 DB 008h, 0C8h

1004 098E 74 DB 009h, 08Eh

1006 0A51 75 DB 00Ah, 051h

1008 0B0F 76 DB 00Bh, 00Fh

100A 0BC4 77 DB 00Bh, 0C4h

100C 0C71 78 DB 00Ch, 071h

100E 0D12 79 DB 00Dh, 012h

1010 0DA7 80 DB 00Dh, 0A7h

1012 0E2E 81 DB 00Eh, 02Eh

1014 0EA5 82 DB 00Eh, 0A5h

1016 0F0D 83 DB 00Fh, 00Dh

1018 0F63 84 DB 00Fh, 063h

101A 0FA6 85 DB 00Fh, 0A6h

101C 0FD7 86 DB 00Fh, 0D7h

101E 0FF5 87 DB 00Fh, 0F5h

1020 0FFF 88 DB 00Fh, 0FFh

1022 0FF5 89 DB 00Fh, 0F5h

1024 0FD7 90 DB 00Fh, 0D7h

1026 0FA6 91 DB 00Fh, 0A6h

1028 0F63 92 DB 00Fh, 063h

102A 0F0D 93 DB 00Fh, 00Dh

102C 0EA5 94 DB 00Eh, 0A5h

102E 0E2E 95 DB 00Eh, 02Eh

1030 0DA7 96 DB 00Dh, 0A7h

1032 0D12 97 DB 00Dh, 012h

1034 0C71 98 DB 00Ch, 071h

1036 0BC4 99 DB 00Bh, 0C4h

1038 0B0F 100 DB 00Bh, 00Fh

103A 0A51 101 DB 00Ah, 051h

103C 098E 102 DB 009h, 08Eh

103E 08C8 103 DB 008h, 0C8h

1040 07FF 104 DB 007h, 0FFh

1042 0736 105 DB 007h, 036h

1044 0670 106 DB 006h, 070h

1046 05AD 107 DB 005h, 0ADh

1048 04EF 108 DB 004h, 0EFh

104A 043A 109 DB 004h, 03Ah

104C 038D 110 DB 003h, 08Dh

104E 02EC 111 DB 002h, 0ECh

1050 0257 112 DB 002h, 057h

1052 01D0 113 DB 001h, 0D0h

1054 0159 114 DB 001h, 059h

1056 00F1 115 DB 000h, 0F1h

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1058 009B 116 DB 000h, 09Bh

105A 0058 117 DB 000h, 058h

105C 0027 118 DB 000h, 027h

105E 0009 119 DB 000h, 009h

1060 0000 120 DB 000h, 000h

1062 0009 121 DB 000h, 009h

1064 0027 122 DB 000h, 027h

1066 0058 123 DB 000h, 058h

1068 009B 124 DB 000h, 09Bh

106A 00F1 125 DB 000h, 0F1h

106C 0159 126 DB 001h, 059h

106E 01D0 127 DB 001h, 0D0h

1070 0257 128 DB 002h, 057h

1072 02EC 129 DB 002h, 0ECh

1074 038D 130 DB 003h, 08Dh

1076 043A 131 DB 004h, 03Ah

1078 04EF 132 DB 004h, 0EFh

107A 05AD 133 DB 005h, 0ADh

107C 0670 134 DB 006h, 070h

107E 0736 135 DB 007h, 036h ; end of table

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137 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

138

139 END

VERSION 1.2h ASSEMBLY COMPLETE, 0 ERRORS FOUND

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DACCON . . . . . . . . . . . . . D ADDR 00FDH PREDEFINED

DACH . . . . . . . . . . . . . . D ADDR 00FCH PREDEFINED

DACL . . . . . . . . . . . . . . D ADDR 00FBH PREDEFINED

DPL. . . . . . . . . . . . . . . D ADDR 0082H PREDEFINED

LED. . . . . . . . . . . . . . . NUMB 00B4H

P3 . . . . . . . . . . . . . . . D ADDR 00B0H PREDEFINED

PLLCON . . . . . . . . . . . . . D ADDR 00D7H PREDEFINED

STEP . . . . . . . . . . . . . . C ADDR 000FH

TABLE. . . . . . . . . . . . . . C ADDR 1000H